Amendments to the Specification:

Please replace the paragraph on page 16, lines 14-26 with the following redlined paragraph:

Fig. 12 illustrates, in the form of functional blocks, a possible structure of a circuit providing a conversion into T. Said circuit converts a value coded on three bits B[2] B[1] B[0] to its transform into T, which transform is coded on seven bits T[7] in T[1], respectively. Said circuit comprises a decoder 901 and six logic elements of OR type, respectively 921~~à~~ to 926. Each bit B[2], B[1], and B[0] is transmitted to decoder 901 which outputs seven values, respectively called is_equal[7], is_equal[6], is_equal[5], is_equal[4], is_equal[3], is_equal[2], is_equal[1]. The output is_equal[1] takes the logical value ' 1 ' when B[2]=' 0 ' and B[1]= ' 0 ' and B[0]=' 1 ' and, in the contrary case, it takes the logical value ' 0 '. Similarly, the outputs is_equal[2], is_equal[3], is_equal[4], is_equal[5], is_equal[6], is_equal[7], take the logical value ' 1 ' when triplet B[2]B[1] B[0] takes the value (0,1,0), (0,1,1), (1, 0, 0), (1,0,1), (1, 1, 0) and (1,1,1), respectively, and the null value in the contrary case.